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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,734	11/27/2000	Keisuke Koga	YAO-432US	2803

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/622,734	KOGA, KEISUKE	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication app ars on the cover sheet with the c rrespondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,9-13 and 17-22* is/are allowed.

6)☒ Claim(s) *1-6 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/01/2003 has been entered.

Response to Amendment

In view of the Request for Continued Examination (Paper No. 16) Amendment C filed 02/10/2003 has been entered (Paper No. 13). In said Amendment C, Applicant substantially amended claims 1, 4, 5 and 7 and added new claims 18-22. Therefore, claims 1-22 are now in the application. Comments on Remarks by Applicant in said Amendment C are included below under "Response to Arguments".

Response to Arguments

Arguments by Applicant as expressed in Remarks contained in Amendment C have been fully considered but are unpersuasive, with the exception of the amendment to claims 7, 8 and 17, as a result of which the objection to said claims 7, 8 and 17 made in Paper No. 12, is herewith withdrawn. Please note, however, that a claim 8 does not further limit device claim 7 (see below under double patenting).

With regard to the Remarks on pages 7-8 on the rejection of claim 1 (from the third paragraph on page 7 on), in Kuriyama extraction electrodes 2 in the (second

preferred) embodiment referred to in the rejection, i.e., Figure 3 rather than Figure 1 to which apparently Applicant refers in his traverse, are positioned higher than gate electrode 8, in accordance with the newly added limitation introduced in claims 1, 4 and 5, said newly added limitation being disclosed in Examples 4, 5, 6 and 7 of the specification: extraction or "grid" electrode 2 and gate ("gate of IGFET") electrode 8 correspond to extraction electrode 48 and gate electrode 49 in Figure 4, extraction electrode 59 and gate electrode 57 in Figure 5; extraction electrode 68 and gate electrode 66 in Figure 6; and extraction electrode 79 and gate electrode 77 in Figure 7, respectively). Therefore, the newly added limitation does not distinguish over the primary reference.

With regard to the traverse of the rejections of claims 2-3, they solely rely on the traverse of the rejection of claim 1.

With regard to the traverse of the rejections of claims 4 and 15 (pages 8-9 of Remarks Amendment C): as detailed above, the gate electrode in Kuriyama et al is positioned lower than the extraction electrode (cf. Figure 3; see also the comments on the traverse of the rejection of claim 1 as included above). Furthermore, although Kawaguchi does not teach an extraction electrode this circumstance is irrelevant to the rejection, because the benefit of preventing hot electrons in his MOSFET through implementing the teaching by Kawaguchi on the gate electrode in the MOSFET incorporated within the field emission cathode apparatus of Kuriyama is relevant to all MOSFETs, regardless of their entourage.

With regard to the traverse of the rejection of claim 6: said traverse entirely rests on the traverse of the independent claim 5 (see comments above on said traverse of the rejection of claim 5).

With regard to the alleged lack of obviousness argument in the rejection of claim 9, the examiner had referred to a section in Hirano ([0029]) in which the relevant aspect of the structure as disclosed by Hirano et al is discussed, as well as its consequence, particularly a stable emission current. However, a closer reading of Hirano shows this teaching not to pertain to the symmetry of the gate electrode as disclosed and claimed, namely in a lateral with respect to the cathode portion of the field emission electron source portion. Therefore, the rejection as based on Kuriyama et al in view of Hirano is withdrawn.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

1. ***Claims 1, 5, 14 and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921).

With regard to claim 1: Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode 2; and

an n-channel field effect transistor portion (comprising IGFET gate electrode 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion, wherein the gate electrode 8 is positioned lower than the extraction electrode 2;

the drain region includes at least two wells 4 and 6 having different impurity concentrations (4 is n-doped and 6 is n+ doped silicon) (cf. column 4, lines 45-46); and

of the at least two wells, one well having a low impurity concentration is provided at an end of the drain (said drain being to the left of the channel

between drain and source; cf, Figure 3) which contacts the channel region of the field effect transistor portion.

Kuriyama et al do not necessarily teach the further limitation that the well having low impurity concentration is provided around a circumference of the other well having a higher impurity concentration. However, as is evidenced by Kojima, it is well known in the art of field effect transistors with insulated gate that the rated voltage can be improved by surrounding the heavily doped drain region by a lightly doped drain region so as to further reduce the gate-drain capacitance; see column 9, lines 1-40 and column 11, line 54 – column 12, line 8). Motivation to include the teaching by Kojima in this regard is the desirability to improve the rated voltage for any insulated gate field effect transistor, including the IGFET in the invention by Kuriyama et al. The inventions can be easily combined through slightly extending the lightly doped drain region. Success in implementing the combination of the teaching by Kojima and the invention by Kuriyama et al can therefore be reasonably expected.

With regard to claim 5: the gate insulation film between the p-silicon substrate 5 and IGFET gate 8 as taught by Kuriyama et al is thinner than the first insulating film 3 (see Figure 3) while the first insulating film is provided between the extraction electrode 2 and the p-type silicon substrate 5, while the gate insulating film is buried with the first insulating film. Thus, with reference to the comments made on claim 1, it is concluded that for exactly the same reasons as given for claim 1 claim 5 is unpatentable over Kuriyama et al in view of Kojima.

With regard to claims 14 and 16: the extraction electrode 2 as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode". Therefore, the further limitations as defined by claims 14 and 16 do not distinguish over the primary reference (Kuriyama et al).

2. ***Claims 2-3*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Kojima as applied to claim 1, and further in view of Akamatsu et al (5,396,096).

As explained above, claim 1 is unpatentable over Kuriyama et al in view of Kojima.

Kuriyama et al nor Kojima necessarily teach the further limitation of claim 2. However, the use of two different impurity elements having different thermal diffusivities or diffusion speeds in the silicon substrate has long been known and applied in the art of field effect transistors, as witnessed by Akamatsu et al, who teach the thermal diffusion of phosphorus and arsenic whose diffusion coefficients are different from each other, phosphorus having a high thermal diffusivity, arsenic having a relatively low thermal diffusivity in the silicon substrate 10 (this remark pertains to claim 3), thus obtaining a heavily doped part and a lightly doped part of the drain (cf. column 11, line 66 – column 12, line 3).

It is well known that the purpose of LDD (lightly doped drain) implementation is the avoidance of hot electron carrier effects (cf. column 11, lines 53-55 in loc. cit.) while the purpose of using different impurities distinct in having different thermal diffusivities is one of obvious convenience: a single heating process establishes two diffusion regions. It is concluded that there is thus motivation to combine the references and that the long-standing success of thermal diffusion for impurity doping combined with the very different thermal diffusivities of phosphorus and arsenic justify a reasonable expectation of success.

3. ***Claims 4 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921) and Kawaguchi (JP401061953A) (as listed in the Information Disclosure Statement of Paper No. 5).

With regard to claim 4: Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

> a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion., while the aforementioned gate electrode 8 is positioned lower than the extraction electrode 2.

Kuriyama et al do not necessarily teach the further limitation that the gate electrode of the field effect transistor portion has a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of near the source region. However, in order to prevent hot carrier generation in a depletion layer of the drain junction, Kawaguchi teaches a gate electrode 1 in a MOS transistor to be wider on the drain side 2 than on the source side 3 (see "Purpose" and "Constitution" in Abstract).

Motivation to include the teaching of Kawaguchi in this regard in the invention by Kuriyama et al stems from the circumstance that suppression of said hot carrier generation would increase the withstand voltage in any MOSFET, irregardless of whether said MOSFET is incorporated into a field emission cathode apparatus of the type essentially taught by Kuriyama et al, while an attempt to achieve an overall

increase the withstand voltage is in line with the objective of Kuriyama et al (see column 1, line 55 – column 2, line 11).

Furthermore, all that is necessary for a *combination* of the inventions is a widening of the gate near the drain. Therefore, *reasonable expectation of success* is justified.

With regard to claims 15: the extraction electrode as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode").

4. ***Claim 6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Kojima as applied to claim 5 above, and further in view of Hirano et al (JP409063467A).

As detailed above, Kuriyama et al anticipate Claim 5; however, they do not necessarily teach the further limitation of Claim 6. Nevertheless, it would have been obvious to use thermal oxidation to produce the insulating film as it is understood in the art that silicon dioxide is an excellent insulating film generally in semiconductor field effect device technology while it is economically produced, given the silicon substrate suitable to provide the fuel, while *Hirano et al teach the use of thermal oxidation of silicon* for the more specific purpose of sharpening the tip of the cathode portion of the field emission electrode source portion of their cold cathode device; see [0034] and title and abstract. *Motivation* to combine stems from the requirement of a micropoint of the

electron emitter taught by Kuriyama et al; see their claim 1 for instance. *Combinability* of the inventions by Kuriyama et al and Hirano et al is obvious in view of the efficiency of producing said tip and gate insulating film together in this manner. *Reasonable expectation of success* of the combination of said inventions follows from the fact that no new steps are introduced at any stage.

Double Patenting

5. ***Claim 8*** is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 7. Please note that the limitation that the shielding electrode must have the same potential as the p-type is already included in claim 7 on which claim 8 depends, while the limitation on the function of said shielding electrode does not add patentable weight within the context of the present device invention. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

6. ***Claims 7 and 17*** are allowable.

7. The following is a statement of reasons for the indication of allowable subject matter: Shielding electrodes in the art of field emission type electron sources with field

effect transistor and made of the same material as the gate electrode, are known in the prior art as witnessed by *Ishikawa et al (JP60124872)*. However, although this teaching would be pertinent to the MOSFET aspect of the invention by Kuriyama et al, said shielding electrode by Ishikawa et al (a) is not held at the same potential as the substrate, and (b) is neither shown nor described to cover a region of the channel. Shielding electrodes with the additional two features (a) and (b) described above have not been found in the Prior Art to date, nor has any reason surfaced as to why such shielding electrodes should be obvious.

8. ***Claims 9-13 and 18-22*** are allowed. The following is a statement of reasons for the indication of allowable subject matter: Although the first portion of claim 9 is taught by Kuriyama, i.e., up to and including line 14 on page 67 of the claim as printed in the disclosure, Kuriyama et al do not teach the further limitation for the drain region (lines 15-18), nor the further limitation for the gate electrode (lines 19-22), the latter with the exception that the gate electrode 8 is positioned lower than the extraction electrode 2, which is taught by Kuriyama et al (see discussion of claim 1). Although Shimomura et al is valid art under 102(a) unless the earliest of the two foreign priority documents is perfected, and although Shimomura et al teach within the context of a MOSFET that the drain 2 should be surrounded by the source region 3 (Figure 1 and page 9, Embodiment 1), and although the teaching by Shimomura et al further includes a symmetrical placement of the gate with respect to the *drain*, both teachings being motivated by the reduction of electric noise through fluctuations particularly for high-frequency

applications (cf. abstract and page 6, line 57 – page 7, line 19 and page 8, lines 5-19), no teaching of a similar nature with regard to a symmetrical placement of the gate with respect to the emission cathode in a field effect device is available. The same comment applies to claim 18, which is taught by Kuriyama et al up to and including line 14 on page 5 of Amendment C, while, with the exception of the teaching by Kuriyama et al of the positioning of the gate electrode at a location lower than the extraction electrode, the further limitations on the drain region of the field effect transistor portion and on the gate electrode of the field effect transistor portion are identical to those in claim 9, and hence the same comment applies to the close but incomplete teaching by Shimomura et al in this regard.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Shimomura et al (EP 0 845 815 A2); Ishikawa et al (JP360124872A).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 4, 2003

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